REMARKS

Claims 1-12, 14-16 are pending. The specification has been amended. Claims 3, 12, and 15 have been amended. No new matter has been added by way of this rejection. Reconsideration and withdrawal of the prior rejections are respectfully requested.

Claims 12-13, 15, and 16 stand rejected as anticipated by U.S. Patent No. 6,292,845 to *Fleck* et al., while claims 1, 2, and 5-7 have been rejected as unpatentable over the same reference in view of U.S. Patent No. 6,317,820 to *Shiell* et al. Claim 14 has been rejected as unpatentable over the *Fleck* et al. patent. Claims 3, 4 and 8-11 have been rejected as unpatentable over the *Fleck* et al. and *Shiell* et al. patents, and further in view of U.S. Patent No. 6,230,180 to *Mohamed* or U.S. Patent No. 5,365,476 to *Mukhanov*. These several rejection are traversed.

Independent claim 12 has been amended to clarify that program code means are defined as including "a sequence of instructions all having the same predetermined bit length". Further that these instructions [of the same predetermined bit length] include "long instructions wherein said predetermined bit length defines a single operation and dual operation instructions wherein said predetermined bit length defines two independent operations". The remainder of claim 12 goes on to define how, among other things, each instruction of said predetermined bit length includes a set of identification bits which are adapted to cooperate with a decode unit to designate whether the instruction is a long instruction or a dual operation instruction.

According to the Examiner, the system disclosed in the *Fleck* patent is capable of executing instructions for two different lengths (namely 16 bit and 32 bit). Applicant must respectfully maintain that the rejection of the claims on this basis is simply incorrect. However, there is a fundamental difference between the claimed computer system and the prior art computer system disclosed in *Fleck*. The claims must be read as a whole to appreciate the true definition of the invention and hence, the features that render the claimed invention patentable over the cited references.

The claimed invention is directed to a computer system employing an instruction stream comprising a sequence of instructions of the same "predetermined length". Among these instructions, there are instructions which define single operations and instructions which define dual operations. The instruction format and decode unit are configured such that the claimed computer system can execute single operations or dual operations, each employing the resources of the computer differently, based on the identification bits within the instruction. As a consequence, only one decode unit and one set of instructions bit per predetermined bit length is needed. This drastically simplifies the fetch decode and instruction semantics required to achieve a given level of performance, while retaining the capability of selecting between levels of instruction parallelism. This novel feature of the invention is recited in all of the independent claims and is not disclosed in any of the cited prior art documents.

With reference to Figure 1 of *Fleck*, therein disclosed is a computer system having instructions of at least two different lengths (see for example col. 1, lines 43-49). After the instructions are retrieved from memory 1, a plurality of instructions is supplied to the instruction buffer 3 via the alignment multiplexer 2. Designated size and type bits in each instruction are tested by instruction length and type

evaluation unit 7. In fact, the significant bit in each instruction indicates the size of the respective instruction (see col. 3, lines 17-19). The evaluation unit 7 checks, through control line 35a, the size of the first instruction in the buffer 3. If the size indicator bit indicates a 16 bit instruction, then the evaluation unit 7 checks line 35b of the second instruction in the instruction buffer. On the other hand, if the size indicator bit indicates a 32 bit instruction, then the evaluation unit 7 uses line 35c to check the size of the second instruction. Significantly, the various instructions in the buffer are delimited by separately probing the length indicator bits and the individual instructions are subsequently passed onwards for separate decoding and execution. Address increment information is passed back to the load instruction 6 via the evaluation unit 7 to correctly increment retrieve addresses through the instruction sequence. From buffer 3, the individual instructions are passed onwards for separate decoding and execution in an appropriate one of the load store and integer pipeline. Because there are separate load store and integer pipelines, instructions of different types can be scheduled to be executed in parallel, whereas instructions of the same kind follow one another on the same pipeline.

Thus, it is apparent that the computer system disclosed in Fleck fails to teach or suggest the use of an instruction of a predetermined bit length to define the alternatives of a single operation or a dual operation task.

U.S. Patent No. 6,317,820 to *Shiell* ("*Sheill*") also fails to teach or suggest the above claimed features of the present invention. Referring to Figure 2 of *Shiell*, therein disclosed is a computer system having CPU 200 having a dual ported program memory 105, an instruction despatch/decode unit 115A, B, A-side and B side execution channels, each comprising a register unit S, an integer unit L, a

multiplier accumulator unit M and a data load store unit D. The data is supplied from a data memory 160 via the register files for side A and side B in a conventionally known manner. *Shiell* uses the term very long instruction word (VILW). Here, the very long instruction word merely comprises a block of 8 single instructions that are simultaneously transferred between certain upstream components to speed up fetching processes (see col. 3, lines 65-66). Accordingly, this architecture can fetch one VILW (or 8 individual instructions) per cycle and supply a maximum of 4 instructions to each of the A and B sides, assuming that each requires a separate functional unit per cycle.

The system disclosed in *Shiell* is directed to supplying additional (duplicate) components so that the computer can support both a first mode of operation and a second mode of operation. In the first mode, the data processor executes a single instruction stream. In the second mode, the data processor executes two independent program instruction streams simultaneously. To do this, fetch/decode circuitry is divided into two parts 115A and 115B each serving a separate side (see for example col. 4, lines 35-44). This permits the CPU to process two instruction streams (each corresponding to half of the VILW 8 instruction packet) simultaneously. Alternatively, the CPU may process a single instruction stream (one half of the 8 instruction very long instruction word packet) in a manner which despatches operations alternately to sides A and B of the processor. See the explanation in the abstract and the paragraph bridging paragraphs 4 and 5 of the specification. As specifically set forth in lines 6 to 11, on each side despatch and decode logic 115A and 115B prepare the half-packets of four individual instructions for execution as per normal. That is, the individual instructions making up each half of the very long instruction word are individually decoded and executed by the appropriate one of units 115A, and 115B. Hence, it is impossible

to conclude that *Shiell* patent teaches or suggests an instruction of a predetermined bit length which is capable of defining either a single operation or a dual operation and having designated identification bits adapted to cooperate with a decode unit to indicate which type of instruction the predetermined bit length defines, and thus fails to cure the deficiency of the *Fleck* et al. patent.

U.S. Patent No. 6,230,180 to *Mohamed* is directed to multiply-accumulate units for use in digital signal processors. According to this reference, each multiply-accumulate unit includes a multiply unit which is coupled with two or more dedicated accumulators (see *Abs.*) However, this reference fails to cure the deficiencies of the *Fleck* et al. patent. Independent claim 8 recites a method that decodes an instruction to detect whether the instruction is a single, operation or two independent operations. When the instruction defines two independent operations, one in each channel, the operations are simultaneously executed, and when the instruction defines a single operation, the channels cooperate to implement a single operation. *Mohamed*, however, teaches simultaneous execution of one single operation, and not of two independent operations within the functional units, as described and claimed. Therefore, the simultaneous execution of dual operations is not taught by *Mohamed*. Accordingly, neither *Fleck*, *Shiell* nor *Mohamed*, either individually or in combination, teach or suggest the invention as claimed, and hence the rejection of the independent claims independent claims 1, 8, 12, and 15 16 are patentantable over the cited references.

In light of the patentability of independent claims 1, 8, amended claims 12, and 15 16, for the reasons above, dependent claims 3-7, 9-11 and 14 are patentable over the prior art.

In light of the foregoing amendments and remarks, this application should be in condition for allowance. Early passage of this case to issue is respectfully requested. However, if there are any

questions regarding this amendment, or the application in general, a telephone call to the undersigned would be appreciated since this expedite the prosecution of the application for all concerned.

Respectfully submitted,

Date: December 20, 2002

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COMPLETE SET OF PENDING CLAIMS

1. A computer system comprising:

a decode unit for decoding instructions fetched from a memory holding a sequence of instructions, all instructions in the sequence having the same predetermined bit length; and

first and second processing channels, each channel comprising a plurality of functional units, at least one of said functional units in each channel being a data processing unit and at least one other of said functional units in each channel being a memory access unit;

wherein the decode unit is operable to detect for each instruction of said predetermined bit length whether the instruction defines a single operation or two independent operations and to control the first and second channels in dependence on said detection.

2. A computer system according to claim 1, wherein, when the decode unit detects that the instruction defines two independent operations, it is operable to control the first channel to implement one of those operations and the second channel to implement the other of those operations, whereby the first and second channels execute their respective independent operations simultaneously.

3. (Amended) A computer system according to claim 1, wherein when the decode unit detects that the instruction defines a single operation, it controls the first and second channels each to cooperate to simultaneously execute said single operation.

4. A computer system according to claim 1, wherein the first and second channels share at least one common register file and can simultaneously access said register file.

5. A computer system according to claim 1, wherein the decode unit is operable to make said detection based on the values of a designated set of identification bits at predetermined bit locations in the instruction.

6. A computer system according to claim 5, wherein, when the instruction has a length of n bits, the predetermined bit locations include the n/2th bit and the nth bit.

7. A computer system according to claim 1, wherein the decode unit is operable to identify certain combinations of said independent operations in an instruction based on said set of identification bits, wherein a first combination denotes two data processing operations, a second combination denotes two memory access operations, a third combination denotes a data processing operation and a memory access operation and a fourth combination denotes a long instruction.

8. A method of operating a computer system which comprises first and second processing channels each having a plurality of functional units including at least one data processing unit and one memory access unit, the method comprising:

decoding an instruction having a predetermined bit length to detect whether that instruction defines a single operation or two independent operations;

where the instruction defines two independent operations, supplying one of the operations to the first processing channel and the other of the operations to the second processing channel whereby the operations are executed simultaneously; and

when the instruction defines a single operation, controlling the first and second processing channels to cooperate to implement said single operation.

9. A method according to claim 8, wherein the step of decoding and detecting comprises reading the values of a designated set of bits at predetermined bit locations in the instruction.

10. A method according to claim 9, wherein said designated bits are used to denote the nature of independent operations when the instruction defines two operations, in addition to designating that the instruction defines a single operation.

11. A method according to claim 8, wherein, for an instruction having n bits, the predetermined bit locations include the n/2th bit and the nth bit.

12. (Twice Amended) A computer program product comprising program code means which include a sequence of instructions all having the same predetermined bit length, said instructions including long instructions wherein said predetermined bit length defines a single operation and dual operation instructions, wherein said predetermined bit length defines two independent operations,

wherein the computer program product is adapted to run on a computer such that a long instruction defining a single operation controls the resources of the computer in a first way and a dual operation instruction defining two independent operations controls the resources of the computer in a second way, and each instruction of said predetermined bit length includes a set of identification bits at designated bit locations within the instruction, said identification bits being adapted to cooperate with a decode unit of a computer system to designate whether the instruction is a long instruction or a dual operation instruction.

14. A computer program product according to claim 13, wherein said designated bit locations in an instruction of n bits include at least n/2th and nth bit.

15. (Amended) A method of operating a computer system which comprises first and second processing channels each having a plurality of functional units including at least one data processing unit and one memory access unit, the method comprising:

fetching a sequence of instructions from a program memory, all said instructions having the same predetermined bit length and containing a set of designated bits at predetermined bit locations within said bit length;

decoding each instruction, said decoding step including reading the values of said designated bits to determine:

a) whether the instruction of said predetermined bit length defines a single operation or two independent operations; and

b) where the instruction of said predetermined bit length defines two independent operations, the nature of each of those operations selected at least from a data processing category of operation and a memory access category of operation.

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Docket No: 3598/0G117

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of: Sophie Wilson

Serial No.: 09/395,294 Art Unit: 2183

Confirmation No.: 5796

Filed: September 13, 1999 Examiner: Stephanie M. Deckter

For: AN INSTRUCTION SET FOR A COMPUTER

MARK-UP FOR AMENDMENT OF DECEMBER 20, 2002
PURSUANT TO 37 C.F.R. §1.121

Box AF
Assistant Commissioner of Patents
Washington, DC 20231

Sir:

IN THE SPECIFICATION:

On page 6, delete the second paragraph and insert the following new second paragraph:

Each register access path 12, 14 carries three addresses from the accessing unit, two source addresses SRC1, SRC2 and a destination address DST. In the case of data processing operations, the source addresses SRC1, SRC2 define registers in the register files 10,11 which hold source operands for processing by the data processing unit. The destination address DST identifies a destination register into which a result of data processing will be placed. The operands and results are conveyed between the register file 10 or 11 and the respective data processing unit via the access paths 12, 14. In the case of load/store operations, the instruction formats allow memory access addresses A_x, A_y to be formulated from data values held in the registers as described in our copending application ([GB-9916566.4] GB-9916564.9, entitled An Instruction Set for a Computer), co-pending U.S. Application Serial No. 09/395,295. The load/store units access a common address space in the form of a data memory 16 via a dual ported data cache DCACHE 15. For this purpose, each load/store unit has a 64 bit data bus Dx,Dy and a 64 bit address bus Ax,Ay.

On page 10, delete the second paragraph and insert the following new second paragraph:

When the decode unit detects the combination denoting a long instruction at bits 29 to 31 and bit 63, the machine operates differently depending on the nature of the instruction. For register/register instruction format L2, the single opcode portion of the 64 bit word is duplicated into the X and Y-channels along path 5_x,5_y to instruct the relevant data processing units in each of the X and Y channels simultaneously to perform the same operation. However, the registers are differently identified, each of the X and Y-channels receiving information identifying their particular registers such that the functional unit in

the X channel accesses its registers (Src1, Src2, Dest1) and the functional unit in the Y channel accesses its registers (Src3, Src4, Dest2). Thus, format L2 in Figure 5 allows register to register data processing. For format [(3)] L3 which allows for register/immediate data processing operations, a 64 bit word identifies a destination register Dest1 and a source register Src1 and defines a 32 bit immediate value. In high and low portions. For the adib/h/w instructions, the immediate value is duplicated to make a 64 bit value which can be added to the 64 bit contents of the source register Src1 and the results loaded into the destination register Dest1.

IN THE CLAIMS:

3. (Amended) A computer system according to claim 1, wherein when the decode unit detects that the instruction defines a single operation, it controls the first and second channels each to cooperate to simultaneously execute [the] said single operation.

12. (Twice Amended) A computer program product comprising program code means which include a sequence of instructions all having the same predetermined bit length, said instructions including long instructions wherein said predetermined bit length defines a single operation and dual operation instructions, wherein said predetermined bit length defines two independent operations, = not means

wherein the computer program product is adapted to run on a computer such that a long instruction ~ change defining a single operation controls the resources of the computer in a first way and a dual

operation instruction defining two independent operations controls the resources of the computer in a second way, and each instruction of said predetermined bit length includes a set [fo] of identification bits at designated bit locations within the instruction, said identification bits being adapted to cooperate with a decode unit of a computer system to designate whether the instruction is a long instruction or a dual operation instruction.

15. (Amended) A method of operating a computer system which comprises first and second processing channels each having a plurality of functional units including at least one data processing unit and one memory access unit, the method comprising:

fetching a sequence of instructions from a program memory, all said instructions having the same predetermined bit length and containing a set of designated bits at predetermined bit locations within said bit length;

decoding each instruction, said decoding step including reading the values of said designated bits to determine:

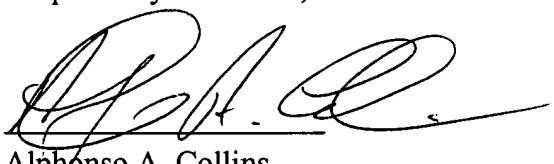
a) whether the instruction of said predetermined bit length defines a single operation or two independent operations; and

b) where the instruction of said predetermined bit length defines two independent operations, the nature of each of those operations selected at least

from a data processing category of operation and a memory access category of operation.

Respectfully submitted,

Date: December 20, 2002



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